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EXAMINER	
DOLLINGER, BRIAN D	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,833	SKRZESZEWSKI ET AL.	
	Examiner	Art Unit	
	Brian D Dollinger	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/4/2002 4/22/2002 7/15/2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Brian Dollinger

DETAILED ACTION

1. This office action is in response to documents received on the following dates: 2/4/2002, 4/22/2002, and 7/15/2002.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) that are not mentioned in the description: Figure 1 and 3 elements 144, 162, and 300. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.83(a) because the drawings in figures 1, 2, and 3 do not have descriptive labels that clearly describe every feature of the invention. Descriptive labels like "insertion module" or "Execution State" are appropriate to include these labels in the drawings to make them more readable and informative. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. Recommended corrections:

5.1. Figure 1: Elements 120, 140, and 160 should be labeled as their different stages, likewise elements 122, 144, and 162 should be labeled or taken out if not relevant, element 180 should be labeled at the Insertion Module, 142 should be labeled as the Detection Module, element 100 should be labeled as a Data Bus.

5.2. Figure 2: Elements 124 should be labeled as it was labeled in figure 1, elements 284 and 282 should have appropriate names like Storage Device and Insertion Control.

5.3. Figure 3: Element 300 should be labeled as Data Bus, elements 320, 340, and 360 should be labeled their appropriate stages, elements 362a-362e should be labeled as Parallel Execution Stages.

6. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Marked-up Drawings" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: A method and system for inserting instructions into a pipeline processor to overcome task switching and error stalls and flushes.

8. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

9. The abstract of the disclosure is objected to because “means” is used in lines 2 and 6 and “said” is used in lines 4 and 10. These words must be removed from the abstract and are not appropriate language for use in the abstract. Correction is required. See MPEP § 608.01(b).

10. The abstract of the disclosure is objected to because at the end of the abstract there is a line, “Figure 1”. This line needs to be removed because the abstract should only be one paragraph. Correction is required. See MPEP § 608.01(b).

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of

the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(e) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(f) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract

and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(g) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(h) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(i) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(j) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property

Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(k) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

11. The disclosure is objected to because of the following informalities: There are no headings to indicate the section in the specification. Headings are needed for the sections: Background of the Invention, Field of the Invention, Description of the Related Art, Brief Summary of the Invention, Brief Description of the Several Views of the Drawings, and Detailed Description of the Invention. Headings included for the Claims and Abstract of the Disclosure need to be more clear and apparent.

Appropriate corrections are required.

Claim Objections

12. Claims 7, 8, 9, 10, and 12 objected to because of the following informalities: In the claims there are reference numbers that refer to elements in the figures. These reference numbers have not effect on the scope of the claim as stated by 608.01(m) in the MPEP. If it is the applicants desire to have the claims limited by the drawings then the applicant should rewrite the claims stating what limitations should be applied without referring to the drawings. Appropriate correction is required. In this office action no weight will be given to the reference numbers in the claims.

Claim Rejections - 35 USC § 112

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 4 and 13 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. Claim 4 recites the limitation "said insertion means" in lines 3 and 4. There is insufficient antecedent basis for this limitation in the claim. For the rest of this office action it is assumed that said insertion means refers to forcing an instruction into the pipeline of the processor from claim 1.

16. Claim 4 contains a reference to said instruction B that has been inserted into said first intermediate pipeline stage by said insertion means in lines 2-4 of the claim. Claim 4 is dependent on claim 1 and claim 1 contains an instruction A and an instruction B. Instruction A in claim 1 is inserted into the first intermediate pipeline stage and instruction B is not being inserted and is the instruction that resides in the second intermediate stage of the pipeline. For the rest of this office action It is assumed that instruction B in claim 4 line 2 is meant to be instruction A and that it is a typo.

17. Claim 13 contains a reference to claim 9 but it is unclear if claim 13 is an independent claim or a dependent claim. It is also unclear what limitations in claim 9 effects the code module in claim 13; if the code module in claim 13 is the instruction bundle in claim 9 or constructed from instruction bundles in

claim 9 and/or other instructions. Further it is unclear if the bit pattern in claim 13 is the same bit pattern described in claim 9.

Claim Rejections - 35 USC § 101

18. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

19. Claim 13 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 13 is directed to non-statutory subject matter because it claims computer code that is not present on any computer readable medium. To fix this change "A computer program product" to "A computer readable program product".

Claim Rejections - 35 USC § 102

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

21. Claims 1-7, 11, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Brown et al. (U.S. 5867701).

22. As per claim 1 Brown et al. taught:

    22.1. A method for manipulating an instruction flow (col. 3 lines 19-22).

22.2. In a pipeline of a processor (Figure 1 showing a pipeline diagram and col. 2 lines 64-65).

22.3. Comprising the following steps: detecting a stimulus leading to a disruption of progress of an instruction through a pipeline (Figures 2 and 3 elements 300 showing the module that detects the stimulus that will slowdown the processor and 310 showing the module that inserts instructions into the pipeline by way of the MUX 320 and the decoder 224 and col. 6 lines 50-54).

22.4. On detecting said stimulus, forcing an instruction (col. 6 lines 60-67).

22.5. Required for responding to said stimulus by said processor directly into a first intermediate pipeline stage (Figure 3 elements 224 shows the first intermediate pipeline stage and 310 shows the module that inserts instructions into the pipeline by way of the MUX 320 and the decoder 224).

22.6. Said intermediate stage becoming available as a result of said disruption (col. 6 lines 65-67). The pipeline stage becomes available because the detection hardware detects the stimulus and then changes the flow of the pipeline accordantly to the stimulus detected. This will stall the pipeline and insert one or more instructions into the pipeline behind or in front of the instruction causing the stimulus.

22.7. Characterized in that said stimulus is detected from an instruction type of an instruction B residing in a second intermediate stage of the

pipeline (col. 6 lines 65-67). After an instruction (instruction B) has cause the detections circuits to signal an inserted instruction (instruction A) instruction B moves on to the next stage into the execution stage or it the instruction was already in the execution stage causing a execution error then the it would stay in the execution stage.

22.8. The stages of a pipeline are assumed to be Fetch, Decode, Execute, and Write-back and the intermediate stages are assumed to be Decode and Execute.

23. As per claim 2, an instruction A (the instruction being inserted by the invention) causing the processor to store a processor status on a stack is inherent to Brown et al.'s invention.

23.1. Brown et al. does not explicitly site how exception would be handled by the invention but exceptions are detected and handled by Brown et al.'s invention (faults and invalid opcodes are types of exceptions, Brown et al. col. 6 lines 51-54 and col. 2 lines 45-47). Brown et al.'s invention refers to the Intel family of processors and their instruction sets as being used with Brown et al.'s invention (Brown et al. col. 2 lines 54-56 and specifically the 486 and Pentium processors col. 4 lines 20-24).

23.2. The Intel manual shows how one of ordinary skill in the art at the time of the invention would handle exceptions in Intel architecture. Exceptions cause the processor to store a processor status on a stack (Intel manual vol. 1 page 4-15 lines 1-4 and Intel manual vol. 1 page 4-16

lines 7-8. The contents of the EFLAGS, CS, and EIP registers are the processor status). An exception would cause the insertion unit to insert an instruction into the pipeline to handle the exception and store a processor status on a stack.

23.3. Processor status is assumed to mean any portion of the processor's registers that can be used to resume an interrupted task.

24. As per claim 3, an instruction A (the instruction being inserted by the invention) causing the processor to retrieve processor status from a stack is inherent to Brown et al.'s invention.

24.1. Brown et al. does not explicitly site how exception would be handled by the invention but exceptions are detected and handled by Brown et al.'s invention (faults and invalid opcodes are types of exceptions, Brown et al. col. 6 lines 51-54 and col. 2 lines 45-47). Brown et al.'s invention refers to the Intel family of processors and their instruction sets as being used with Brown et al.'s invention (Brown et al. col. 2 lines 54-56 and specifically the 486 and Pentium processors col. 4 lines 20-24).

24.2. The Intel manual shows how one of ordinary skill in the art at the time of the invention would handle an exception return in Intel architecture. Exception returns cause the processor to retrieve processor status on a stack (Intel manual vol. 1 page 4-16 lines 19-20 and Intel manual vol. 1 page 4-16 lines 26-27. The contents of the EFLAGS, CS, and EIP registers are the processor status and are assumed to be on the

stack because of the way exceptions are called as stated above). An exception return would cause the insertion unit to insert an instruction to retrieve a process status from the stack.

24.3. Processor status is assumed to mean any portion of the processor's registers that can be used to resume an interrupted task.

25. As per claim 4, Brown et al. taught that instruction A (the instruction being inserted by the invention) is an interrupt call that has been inserted into said first intermediate pipeline stage by said insertion means. Brown et al. taught that their invention would receive user input through the code breakpoint circuit figure 5 element 520 such as a keyboard input (Brown et al. col. 9 lines 52-54). Keyboard input is processed by using a hardware interrupt. Input from a keyboard would cause the insertion unit to insert an I/O interrupt into the pipeline.

26. As per claim 5 Brown et al. taught that instruction B (the instruction causing the disturbance) is a programmable instruction causing a pipeline flush.

26.1. Brown et al. does not explicitly site how exception would be handled by the invention but exceptions are detected and handled by Brown et al.'s invention (faults and invalid opcodes are types of exceptions, Brown et al. col. 6 lines 51-54 and col. 2 lines 45-47). Brown et al.'s invention refers to the Intel family of processors and their instruction sets as being used with Brown et al.'s invention (Brown et al. col. 2 lines 54-56 and specifically the 486 and Pentium processors col. 4 lines 20-24).

26.2. The Intel manual shows how one of ordinary skill in the art at the time of the invention would handle exceptions in Intel architecture. An exception would cause a pipeline flush (Intel manual vol. 3 table A-2 on page A-14 row 8 col. 2 and 3).

27. As per claim 6 Brown et al. taught that instruction A (the instruction being inserted by the invention) causes the processor to store a return address on a stack.

27.1. Brown et al. does not explicitly site how exception would be handled by the invention but exceptions are detected and handled by Brown et al.'s invention (faults and invalid opcodes are types of exceptions, Brown et al. col. 6 lines 51-54 and col. 2 lines 45-47). Brown et al.'s invention refers to the Intel family of processors and their instruction sets as being used with Brown et al.'s invention (Brown et al. col. 2 lines 54-56 and specifically the 486 and Pentium processors col. 4 lines 20-24).

27.2. The Intel manual shows how one of ordinary skill in the art at the time of the invention would handle exceptions in Intel architecture. An exception would cause a pipeline flush (Intel manual vol. 3 table A-2 on page A-14 row 8 col. 2 and 3) and it would store a return address on a stack by storing the CS and EIP registers (Intel manual vol. 3 page 5-15 lines 20-23) and exception.

28. As per claim 7 Brown et al. taught:

28.1. A system for manipulating an instruction flow (col. 3 lines 19-22).

28.2. Comprising: a processor having a processing pipeline (Figure 1 showing a pipeline diagram and col. 2 lines 64-65).

28.3. Detection means for detecting a stimulus leading to a disruption of the progress of an instruction through said pipeline (Figures 2 and 3 elements 300, showing the module that detects the stimulus that will slowdown the processor and 310 showing the module that inserts instructions into the pipeline by way of the MUX 320 and the decoder 224 and col. 6 lines 50-54).

28.4. Insertion means, responsive to said detection means (Figure 3 element 310 as indicated the module that inserts instructions in to the pipeline).

28.5. For forcing an instruction A directly into a first intermediate pipeline stage (Figure 3 elements 224 shows the first intermediate pipeline stage and 310 shows the module that inserts instructions into the pipeline by way of the MUX 320 and the decoder 224). The insertion module 221 inserts the instructions into the decode stage of the pipeline this being the first intermediate pipeline stage.

28.6. Said stage becoming available as a result of said disruption, characterized in that said stimulus is detectable from an instruction type of an instruction B (Figure 3 element 300 shows the detection circuits and col. 6 lines 51-54). The pipeline stage becomes available because the detection hardware detects the stimulus and then changes the flow of the pipeline accordantly to the stimulus detected. This will stall the pipeline

and insert one or more instructions into the pipeline behind or in front of the instruction causing the stimulus.

28.7. Residing in a second intermediate stage of the pipeline (col. 6 lines 65-67). After an instruction (instruction B) has cause the detections circuits to signal an inserted instruction (instruction A) instruction B moves on to the next stage into the execution stage or it the instruction was already in the execution stage causing a execution error then the it would stay in the execution stage.

28.8. The stages of a pipeline are assumed to be Fetch, Decode, Execute, and Write-back and the intermediate stages are assumed to be Decode and Execute.

29. As per claim 11 Brown et al. taught that the instruction to be forced into a pipeline by said insertion means is present in the system in a hard-coded manner (col. 7 lines 36-40 and 49-51).

30. As per claim 12 Brown et al. taught that the instruction to be forced into a pipeline by said insertion means is stored in a data storage device (col. 7 lines 37-40 and 49-51).

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. Claims 8-10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. as applied to claim 7 above, and further in view of Miller (U.S. 6081884).

33. As per claim 8 Brown et al. taught:

33.1. Pipeline comprises a plurality of execute stages for executing the plurality of instructions of said instruction bundle in a parallel fashion (Figure 2 element 280 and col. 6 lines 31-37).

33.2. Detections means precedes the plurality of execute stages (Figure 2 element 221 and 280).

33.3. However Brown et al. does not teach that Instruction B (the instruction causing the disturbance) is an element of an instruction bundle comprising a plurality of instructions.

33.4. Brown et al.'s invention is not a VLIW or LIW architecture, it is an X86 architecture. If Brown et al.'s invention was a VLIW or LIW architecture then the detection unit would detect a disturbance caused by one of the instructions in the bundle.

33.5. Miller taught the use of the X86 instruction set in a LIW format (col. 1 lines 60-63 and Figure 2 showing multiple instructions bundled together to make one long instruction) in which more then one instruction is contained in each instruction bundle (col. 1 lines 67, col. 2 lines 1-3, and Figure 2). This was done to gain performance by exploiting more

parallelism (col. 2 lines 7-9) while utilizing the vast amount of code already written for the X86 architecture (col. 2 lines 30-35).

33.6. The gain in performance through exploiting more parallelism using a LIW format along with the large amount of code already written for X86 processors would have motivated one skilled in the art at the time of the invention to combine Brown et al.'s invention with the teachings of Miller to utilize instruction bundles containing multiple instructions in the LIW architecture.

34. As per claim 9 Brown et al. taught the detection means is arranged to evaluate a bit pattern attached to the instruction, with the combination of Brown et al. with Miller from claim 8 the instruction will become an instruction bundle (col. 2 lines 55-56) and a bit pattern marking the presence of said instruction type amongst said plurality of instructions (col. 2 lines 55-56). Brown et al. sites the use of special instruction prefixes that can be used to identify instructions that would be detected this prefix would inherently be directed to specific instruction in the instruction bundle.

35. As per claim 10 Brown did not teach that the instruction bundle in claim 8 was a Very Long Instruction Word (VLIW).

35.1. Miller taught the use of the X86 instruction set in a LIW format (col. 1 lines 60-63 and Figure 2 showing multiple instructions bundled together to make one long instruction) in which more then one instruction is contained in each instruction bundle (col. 1 lines 67, col. 2 lines 1-3, and Figure 2). This was done to gain performance by exploiting more

parallelism (col. 2 lines 7-9) while utilizing the vast amount of code already written for the X86 architecture (col. 2 lines 30-35).

35.2. The gain in performance through exploiting more parallelism using a LIW format along with the large amount of code already written for X86 processors would have motivated one skilled in the art at the time of the invention to combine Brown et al.'s invention with the teachings of Miller to utilize instruction bundles containing multiple instructions in the LIW architecture.

35.3. The LIW format used in Miller is the same instruction format that Skrzeszewski et al. uses in their application. LIW and VLIW instruction formats refer to the same type of architecture in this case.

36. As per claim 13 Brown et al. taught:

36.1. A computer program product comprising a code module for execution by the system of claim 9 (the combination of Brown et al. and Miller's system inherently has code that runs on the system).

36.2. Characterized in that said code module comprises an instruction extended with a bit pattern (col. 2 lines 55-56, special instruction prefixes).

36.3. Said bit pattern making said instruction recognizable to the detection means of one of said systems (col. 8 lines 40-42).

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian D Dollinger whose telephone number is (703) 305-8978 or (571) 272-4164. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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